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| 10/584,158 | 06/22/2006 | Yong-Sung Jeon | CU-4896 WWP | 5062 |

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| EXAMINER | |
|---|---|
| SANDIFER, MATTHEW D | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/584,158 | JEON ET AL. | |
| | Examiner | Art Unit | |
| | MATTHEW SANDIFER | 2193 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 June 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-7 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to the amendment filed 6/24/2010.

2. Claims 1, 3-7, and 9-12 are pending in this application. Claims 2 and 8 are cancelled by way of amendment. Claims 1 and 7 are independent claims. This Office Action is made final.

### *Examiner Notes*

3. Examiner cites particular columns and line numbers in the references as applied to the claims below for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested that, in preparing responses, the applicant fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

### *Claim Objections*

4. Claim 3 is objected to because of the following informalities: the claim depends from cancelled claim 2. Examiner interprets the claim to be dependent on independent claim 1. Appropriate correction is required.

5. Claim 9 is objected to because of the following informalities: the claim depends from cancelled claim 8. Examiner interprets the claim to be dependent on independent claim 7. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-5 and 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oerlemans (US 6,807,553) in view of Tran et al. (US 6,356,112) (hereinafter Tran).

As per Claim 1, Oerlemans discloses an apparatus for generating random numbers using digital logic (Column 1, lines 53-54, a digital circuit generates true random numbers); comprising a shift register which sequentially moves bit values stored therein (Figure 2 and Column 4, lines 1-8, circuit comprises a linear feedback shift register that shifts bit values through delay stages); a feedback circuit which performs a first predetermined logic operation on the bit values stored in the shift register to generate a feedback signal, and which performs a predetermined logic operation on the feedback signal and the external signal and inputs a result of operation to the shift register (Figure 2 and Column 3, lines 60-65 and Column 4, lines 1-8, the feedback function is implemented by multiple-input XOR feedback circuit; multiple-input XOR circuit additionally accepts external random signal as input and outputs result to input of LFSR); an external signal generation circuit which generates an external signal input to the shift register (Figure 1 and Column 3, lines 22-24 and 60-65, the oscillator sampling circuit produces random noise signal 1a that is input to the LFSR at input 2a); and a fixed value prevention

circuit that generates a signal with a value that allows an output of the input logic circuit to have a different value to a value of an output of the shift register and inputs the generated signal to the input logic circuit when a logic value of the external signal is equivalent to all the bit values stored in the shift register (Figure 2 and Column 4, lines 8-20, the NOR feedback circuit generates a logic 1 signal input to the multiple-input XOR circuit when the LFSR state is all logic 0 and thus the LFSR feedback signal is logic 0, which generates a logic 1 signal output of the XOR circuit and input to the LFSR when the input random bit signal is logic 0 and the LFSR state is all logic 0).

Oerlemans does not explicitly disclose an input logic circuit, separate from the feedback circuit, which performs a second predetermined logic operation on the feedback signal and the external signal, and inputs a result of operation to the shift register, and wherein the external signal is directly connected to the input logic circuit.

However, Tran discloses a multiple-input XOR gate comprises multiple logic circuits (Figure 5 and Column 7, lines 10-19, an N-input XOR gate is comprised of multiple 2-input XOR circuits); and therefore discloses an input logic circuit, separate from the feedback circuit, which performs a second predetermined logic operation on the feedback signal and the external signal, and inputs a result of operation to the shift register, and wherein the external signal is directly connected to the input logic circuit (Oerlemans, Figure 2, the feedback loops of Oerlemans are XOR'd, which is further XOR'd with the external signal 2a; Tran, Figure 5, the multiple feedback loops are XOR'd by a feedback circuit, i.e. the XOR circuits labeled 12 in Figure 5 of Tran, and input to an input logic circuit, i.e. the final 3-input XOR comprising the final stage 12 and stage 14 of Tran, wherein the input logic circuit accepts the XOR'd feedback

signal, the fixed value prevention signal, and the external signal directly as input, and wherein the result of the input logic circuit, i.e. 3-input XOR circuit, is input directly to the shift register as shown in Figure 2 of Oerlemans).

Oerlemans and Tran are analogous art because both are directed to digital circuit implementations utilizing XOR gates.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the multiple-input XOR implementation of Tran to the teachings of Oerlemans because it provides a fast and small XOR circuit architecture (Column 4, lines 8-19, the implementation provides an improved balance between circuit size and performance over previous designs).

As per Claim 3, Oerlemans discloses the apparatus of claim 1, wherein the signal output from the fixed value prevention circuit is at logic high (Column 4, lines 8-20, the NOR feedback circuit generates a logic 1 signal input to the multiple-input XOR circuit when the LFSR state is all logic 0).

As per Claim 4, Oerlemans disclose the apparatus of claim 1, wherein the external signal generation circuit generates a random signal (Column 2, lines 4-23, the free running oscillators are sampled to generate a random noise signal).

As per Claim 5, Oerlemans discloses the apparatus of claim 4, wherein the random signal is generated by sampling a sampled signal generated by a source that is different from a source

of a sampling signal (Figure 1 and Column 2, lines 35-42 and Column 3, lines 37-44, the random noise signal is generated by sampling the signal generated by the free-running oscillators according to a separate system clock signal).

As per Claim 7, Oerlemans discloses a method of generating random numbers using digital logic (Column 1, lines 7-10, the circuit implements a technique of generating random numbers); comprising (a) sequentially moving bit values stored in a shift register (Figure 2 and Column 4, lines 1-8, a linear feedback shift register shifts bit values through delay stages); (b) performing a predetermined logic operation on the bit values stored in the shift register (Figure 2 and Column 4, lines 1-8, the feedback function is implemented by performing XOR on values stored in the shift register); (c) generating an external signal input to the shift register (Figure 1 and Column 3, lines 60-65, the oscillator sampling circuit produces random noise signal that is input to the LFSR); and (d) performing a predetermined operation on the feedback signal and the external signal and inputting a result of the operation to the shift register (Figure 2 and Column 3, lines 60-65 and Column 4, lines 1-8, multiple-input XOR circuit performs XOR on feedback signals and external random signal, and outputs result to input of LFSR); and wherein the predetermined logic operation is further performed on an output of a fixed value prevention circuit that allows the result of the predetermined logic operation to be different to the bit values of the shift register, when a logic value of the external signal is equivalent to all the bit values stored in the shift register (Figure 2 and Column 4, lines 8-20, the NOR feedback circuit generates a logic 1 signal input to the multiple-input XOR circuit when the LFSR state is all logic 0 and thus the LFSR feedback signal is logic 0, which generates a logic 1 signal output of

the XOR circuit and input to the LFSR when the input random bit signal is logic 0 and the LFSR state is all logic 0); and wherein the external signal and the output of the fixed value prevention circuit are directly inputted into the predetermined logic operation (Figure 2, external signal 2a and output from the NOR circuit 7 are directly input to the XOR operation 6).

Oerlemans does not explicitly disclose performing a predetermined operation to generate a feedback signal and separately performing a predetermined operation on the feedback signal and the external signal.

However, Tran discloses a multiple-input XOR gate comprises multiple logic circuits (Figure 5 and Column 7, lines 10-19, an N-input XOR gate is comprised of multiple 2-input XOR circuits; therefore the multiple input XOR circuit of Oerlemans first generates a feedback signal via the XOR circuits labeled 12 in Figure 5 of Tran, and subsequently performs an XOR operation on the feedback signal and the external signal, via the final 3-input XOR comprising the final stage 12 and stage 14 of Tran).

Oerlemans and Tran are analogous art because both are directed to digital circuit implementations utilizing XOR gates.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the multiple-input XOR implementation of Tran to the teachings of Oerlemans because it provides a fast and small XOR circuit architecture (Column 4, lines 8-19, the implementation provides an improved balance between circuit size and performance over previous designs).

As per Claim 9, Oerlemans discloses the method of claim 7, wherein the output of the fixed value prevention circuit is at logic high (Column 4, lines 8-20, the NOR feedback circuit generates a logic 1 signal input to the multiple-input XOR circuit when the LFSR state is all logic 0).

As per Claim 10, Oerlemans discloses the method of claim 7, wherein the external signal is a random signal (Column 2, lines 4-23, the free running oscillators are sampled to generate a random noise signal).

As per Claim 11, Oerlemans discloses the method of claim 10, wherein the random signal is generated by sampling a sampled signal generated by a source that is different from a source of a sampling signal (Figure 1 and Column 2, lines 35-42 and Column 3, lines 37-44, the random noise signal is generated by sampling the signal generated by the free-running oscillators according to a separate system clock signal).

4. Claims 6 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oerlemans in view of Tran, and further in view of Tamamura et al. (US 5,001,361) (hereinafter Tamamura).

As per Claim 6, the apparatus of claim 5 is disclosed as described above.

Oerlemans in view of Tran does not explicitly disclose wherein sampling is performed both at rising and falling edges of the sampling signal generated by a source that is different from a source of the sampled signal.

However, Tamamura discloses wherein sampling is performed both at rising and falling edges of the sampling signal generated by a source that is different from a source of the sampled signal (Column 7, lines 21-26 and 34-39, a flip flop circuit samples the data input on the rising and falling edge of the system clock signal).

Oerlemans and Tamamura are analogous art because both are directed to digital circuit implementations utilizing flip flops.

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the flip flop circuit implementation of Tamamura to the sampling D-flip flop of Oerlemans because it provides for fast, non-erroneous operation (Column 7, lines 47-53, implementation is high-speed and eliminates erroneous operation).

As per Claim 12, the method of claim 11 is disclosed as described above.

Oerlemans in view of Tran does not explicitly disclose wherein sampling is performed both at rising and falling edges of the sampling signal generated by a source that is different from a source of the sampled signal.

However, Tamamura discloses wherein sampling is performed both at rising and falling edges of the sampling signal generated by a source that is different from a source of the sampled signal (Column 7, lines 21-26 and 34-39, a flip flop circuit samples the data input on the rising and falling edge of the system clock signal).

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the flip flop circuit implementation of Tamamura to the sampling D-flip flop of Oerlemans because it provides for fast, non-erroneous operation (Column 7, lines 47-53, implementation is high-speed and eliminates erroneous operation).

***Response to Arguments***

7. Applicant's arguments filed 6/24/2010 have been fully considered but they are not persuasive.

a. Applicant argues on pages 6-7 and 10 for amended independent claims 1 and 7 that the cited references by Oerlemans, Tran, and/or Tamamura fail to disclose directly inputting an external signal, a single feedback signal, and a signal generated by a fixed value prevention circuit to the input logic circuit, and wherein the external signal is directly connected to the input logic circuit, as recited in the amended independent claims.

The Examiner respectfully submits that Oerlemans teaches an external signal, i.e. the signal 2a in Figures 1 and 2, and a fixed value prevention circuit, i.e. NOR circuit 7, wherein the external signal and the signal generated by the fixed value prevention circuit are both directly connected to XOR circuit 6. Oerlemans additionally teaches XOR'ing a plurality of feedback loops with the external signal and the signal generated by the fixed value prevention circuit. Furthermore, Tran teaches a multiple-input XOR gate comprises multiple logic circuits, wherein the feedback loops of Oerlemans are first

XOR'd by circuits labeled 12 in Figure 5, and wherein the final circuits labeled 12 and 14 yields a three-input XOR circuit, i.e. the input logic circuit. Once the feedback loops have been XOR'd to generate a single signal i.e. the feedback signal, the feedback signal, external signal, and fixed value prevention signal are directly input to the three-input XOR and the result is output to the shift register as shown in Oerlemans, Figure 2.

b. Applicant argues on pages 7-8 and 10 for amended independent claims 1 and 7 that Oerlemans can not disclose directly inputting an external signal, a single feedback signal, and an output from the NOR circuit 7 of Oerlemans to the input logic circuit, such that the XOR circuit 6 of Oerlemans generates a different value to a value of an output of the shift register, when a logic value of the external signal is equivalent to all the bit values stored in the shift register.

The Examiner respectfully submits that the NOR circuit 7 of Oerlemans generates a logic 1 when the bit values in the shift register, and the output of the shift register, are all logic 0. Furthermore, the XOR of all feedback loops generates a logic 0 when the bit values in the shift register, and the output of the shift register, are all logic 0. When the external signal is equivalent to all the bit values stored in the shift register = 0, the XOR of the feedback signal = 0, and the NOR output = 1, and the external signal = 0, generates a logic 1. Thus the XOR circuit 6 of Oerlemans, wherein the XOR circuit 6 is the input logic circuit when combined with Tran as described above, generates a different value (logic 1) to the value of an output of the shift register (logic 0), such that the shift register does not stall in a state of all logic 0's.

c. Applicant argues on pages 8-9 that Figure 3 of the instant application illustrates a fixed value prevention circuit that prevents series generated by a shift register from being unchanged in response to clock input, and argues that the presently claimed invention discloses being able to randomly generate every possible complete random number that can be statistically generated according to a bit value and using only digital logic.

In response to applicant's argument, it is noted that these features upon which applicant relies are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

***Conclusion***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 7,206,797 Random number slip and swap generators, discloses a random number generator comprising a shift register, feedback circuit, direct external signal input, input logic circuit, and fixed value prevention circuit

US 2004/0049525 Feedback random number generation method and system, discloses LFSR random number generator with feedback circuit and fixed value prevention circuit

US 6,687,721 Random number generator with entropy accumulation, discloses LFSR random number generator with feedback circuit and fixed value prevention circuit

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW SANDIFER whose telephone number is (571) 270-5175. The examiner can normally be reached on 8:30am - 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/M. S./
Examiner, Art Unit 2193

/Chat C. Do/
Primary Examiner, Art Unit 2193